IJREAT International Journal of Research in Engineering & Advanced Technology, Volume 2, Issue 2, Apr-May, 2014
ISSN: 2320 – 8791(Impact Factor: 1.479)
www.ijreat.org

Design & Implementation Of Address Generation Circuit Of IEEE 802.16e Deinterleaver Using FPGA

Pradeep N[1], Smt. H Umadevi[2]

[1]PG Student, Department of Electronics & Communication, Dr. Ambedkar Institute of Technology, Bangalore, India.
[2]Associate. Professor, Department of Electronics & Communication, Dr. Ambedkar Institute of Technology, Bangalore, India.

***Abstract*—Improvements in mobile communication and broadband have provided many advantages to its subscribers, like high-speed internet and high-quality video and voice application services. WIMAX is a outstanding technology that provides broadband to "last mile" scenarios. It offers both line of Sight and non-line of sight wireless communication. In this paper, an optimized technique is proposed for FPGA implementation of the address generation circuit of the Wimax deinterleaver block which includes quadrature phase-shift keying (QPSK), 16-quadrature-amplitude modulation (QAM), and 64-QAM modulation techniques.**

***Keywords*—Address generator, WiMAX,Deinterleaver, Verilog, Field Programmable gate Arrays(FPGA)**

I. INTRODUCTION

Few decades ago, we were purely dependent on analog system. The sources and transmission system were on analog format but the development of technology made it possible to transmit data in digital form. Along with those, improvement from wire to wireless concept emerged and after researching and investing so much money, engineers became successful to invent wireless transmitter to transmit data. Applications like internet access, instant messaging, voice, SMS, paging, file transferring, video conferencing, entertainment and gaming etc became a part of life.

WIMAX IEEE 802.16e was an amendment of 802.16d standard which finished in 2005 and known as 802.16e-2005. Its main endeavor is mobility including large range of coverage. Sometimes it is called mobile WIMAX. This standard is a technical updates of fixed WIMAX which has robust support of mobile broadband. The IEEE 802.16e standard, commonly known as mobile Wimax, is the latest wireless technology that has promised to offer Broadband Wireless Access over long distance. The air interface is found to be the interface for the next generation broadband Wireless System. In this paper, we present a method to model the Address Generation circuitry of WiMAX interleaver using Verilog on FPGA platform with all code rates and modulation schemes of IEEE 802.16e standard. Our technique provides better performance in terms of maximum operating frequency, use of flip-flops with negligible loss in terms of logic cells utilized compared to existing FPGA based implementations. Measured circuit parameters and software simulation of this model are also provided**.** In paper [1] we get the methodology required for the FPGA implementation of deinterleaver block. Work in [2] describes about grouping of incoming data streams into the block. Work in [3] gives the idea for hardware description language VHDL based implementation of address generator with ½ code rate. In paper [1] we get the methodology required for the FPGA implementation of deinterleaver block. Work in [2] describes about grouping of incoming data streams into the block. Work in [3] gives the idea for hardware description language VHDL based implementation of address generator with ½ code rate.

The system level overview of IEEE 802.16e based WiMAX system is described in Fig.1.In this system, the input stream which is in binary form, obtained from the source is randomized in order to prevent the long series of 1s and 0s,which causes timing problem at the receiver side. Then the data bits are encoded using Reed Solomon (RS) encoder and Convolutional Coder (CC). The former is suitable for correction of burst type of error whereas the later is for random error. After RS-CC encoding all encoded data bits are interleaved by a block interleaver. In traditional block interleaver bits received from the encoder are stored row wise in the interleaver's memory. As soon as the memory is completely filled, the bits are read column-by-column manner. After interleaving, data passes through the mapper block in which modulation takes place. The resulting data symbols are used to construct one symbol by performing Inverse Fast Fourier Transform (IFFT). Cyclic Prefix (CP) is used to reduce ISI and ICI. In the receiver, inverse blocks are applied which perform DFT, demapping, deinterleaving, decoding and derandomizing operations in sequential manner to get back the original data bits.

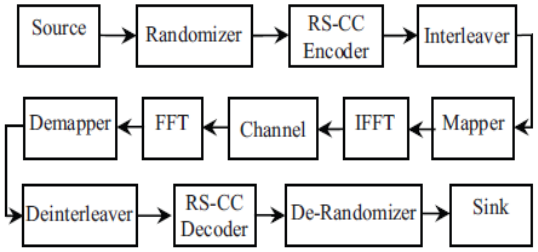


Fig 1.Wimax transceiver Block diagram

II. PROPOSED METHOD

Proposed method includes modification in the circuit of deinterleaver which contains qpsk block, 16-QAM block and 64-QAM when compared to the previous methodology [1], where there were comparators, which are used to reset the column counter and row counter. But in our design we omitted the comparators and the column counters and row counters are reset by using the reset input and hence the extra hardware required to implement the reset for the comparators in QPSK,16-QAM and 64-QAM is omitted and all other resources are utilized as in [1].

A. INTERLEAVING IN WIMAX SYSTEM

The block interleavers used in WiMAX system have dissimilar interleaving pattern for different code rates and modulation schemes. A variety of interleaver depths are required to incorporate various code rates and modulation schemes. Table I describes permitted interleaver depths in IEEE 802.16e for all code rates and modulation schemes. The encoded bits are interleaved using two step process. The first step ensures that the adjacent coded bits are mapped onto nonadjacent subcarriers, which provides frequency diversity and improves the performance of the decoder. The second step ensures that adjacent bits are alternately mapped to less and more significant bits of the modulation constellation to avoid long run of lowly reliable bits.

B. INTERLEAVER ADDRESS GENERATION

The values of j_k obtained from (2) are the write addresses of interleaver memory. On evaluation of (1) and (2) with Ncbps = 96 (. code rate, QPSK), Ncbps = 288 (. code rate, 16-QAM) and with Ncbps = 384 (⅔ code rate, 64-QAM) we find all the values of jk, out of which first 32 values are listed in Table II. On careful examination of the values of jk, it has been found that the subsequent addresses are not equally spaced for all cases. Within a modulation scheme, the increment values follow a fixed type of pattern irrespective of coding rate.. In case of QPSK (with s = 1) the increments are linear having values like 6 for Ncbps = 96, 9 for Ncbps = 144 and so on. 16-QAM (with s = 2) and 64-QAM (with s = 3) have nonlinear increments like 13, 11 for Ncbps = 192 and 20, 17, 17 for Ncbps = 288 respectively.

Let Ncbps is the block size corresponding to the number of coded bits per allocated sub-channels; d represents number of columns of the block interleaver which is typically chosen to be 16 for WiMAX. m_k is the output after first level of permutation and k varies from 0 to Ncbps -1. s is a parameter defined as s= Ncpc/2, where Ncpc is the number of coded bits per sub-carrier, i.e., 2, 4 or 6 for QPSK, 16-QAM or 64-QAM respectively .

The first and second levels of permutation are given by (1) and (2) respectively are as follows:

$$m_k = \left(\frac{N_{cbps}}{d}\right)(k\%d) + \left\lfloor \frac{k}{d} \right\rfloor \quad (1)$$

$$j_k = s\times\left\lfloor \frac{m_k}{s} \right\rfloor + \left(m_k + N_{cbps} - \left\lfloor \frac{d \times m_k}{N_{cbps}} \right\rfloor\right)\%s \quad (2)$$

C. DEINTERLEAVER ADDRESS GENERATION

The deinterleaver, which performs the inverse operation, is also defined by two permutations, i.e., (3) and (4). Let m_j and k_j define the first and second level of permutations for the deinterleaver, where j is the index of received bits within a block of N_{cbps} bits. (3) And (4) perform inverse operation of (2) and (1), respectively. Thus

$$m_j = s\cdot\left\lfloor \frac{j}{s} \right\rfloor + \left(j + \left\lfloor \frac{d.j}{N_{cbps}} \right\rfloor\right)\%s \quad (3)$$

$$k_j = d.m_j - (N_{cbps} - 1)\cdot\left\lfloor \frac{d.m_j}{N_{cbps}} \right\rfloor. \quad (4)$$

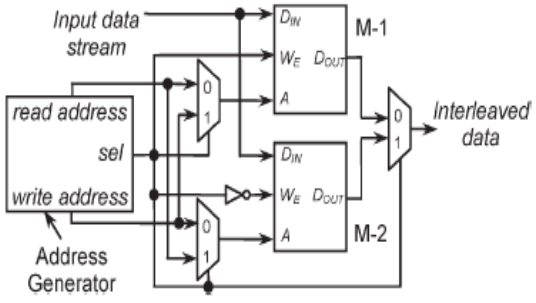


Fig 2.Circuit diagram for interleaving/deinterleaving

TABLE I
PERMITTED INTERLEAVER/DEINTERLEAVER DEPTH IN IEEE 802.16e FOR ALL CODE RATES AND MODULATION SCHEMES

Modulation Scheme	QPSK (s=1)		16-QAM (s=2)		64-QAM (s=3)		
Code Rate	½	¾	½	¾	½	⅔	¾
Interleaver Depth, N_{cbps} in bits	96	144	192	288	288	384	432
	192	288	384	576	576	-	-
	288	432	576	-	-	-	-
	384	576	-	-	-	-	-
	480	-	-	-	-	-	-
	576	-	-	-	-	-	-

TABLE II
FIRST FOUR ROWS AND FIVE COLUMNS OF DEINTERLEAVER SAMPLE ADDRESSES FOR THREE CODE RATES AND MODULATION TYPES

N_{cbps}, code rate and modulation type	De-interleaver addresses				
N_{cbps} = 96-bits, ½ code rate, QPSK	0	16	32	48	64
	1	17	33	49	65
	2	18	34	50	66
	3	19	35	51	67
N_{cbps} = 192-bits, ½ code rate, 16-QAM	0	16	32	48	64
	17	1	49	33	81
	2	18	34	50	66
	19	3	51	35	83
N_{cbps} = 576-bits, ¾ code rate, 64-QAM	0	16	32	48	64
	17	33	1	65	81
	34	2	18	82	50
	3	19	35	51	67

D. TRANSFORMATION INTO CIRCUIT

In order to test the proposed algorithms for the address generator of the WiMAX deinterleaver with all modulation schemes, transformations of these algorithms into digital circuits is made and are shown in Fig. 3(a)–(c). The QPSK hardware shown in Fig. 3(a) has a row counter RWC0 to generate row numbers between 0 and $d - 1$. A column counter CLC0 with multiplexer M0 and comparator C0 generate the variable column numbers to implement permissible N_{cbps}. A multiplier ML0 and an adder A0 perform the desired operations to implement (5). The address generator for 16-QAM follows a similar structure, such as that of QPSK with few additional modules. These modules are designed with an incrementer, a decrementer, two modulo-2 blocks, and two multiplexers, as shown in Fig. 3(b).

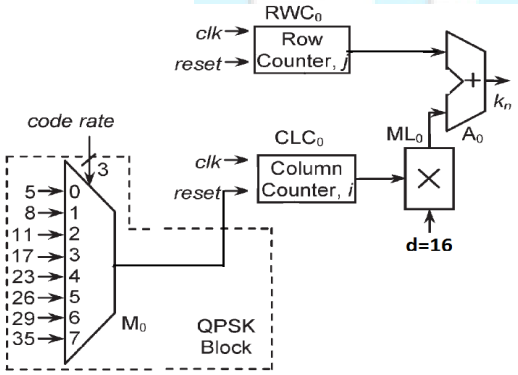
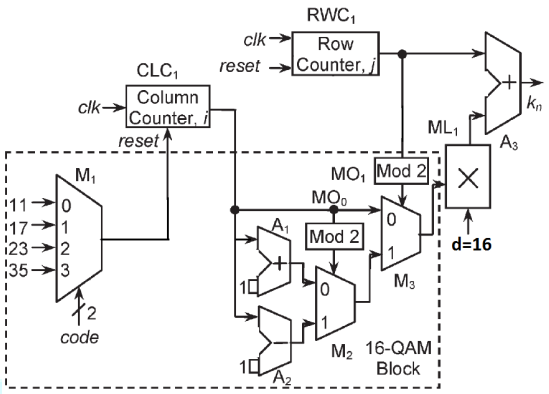
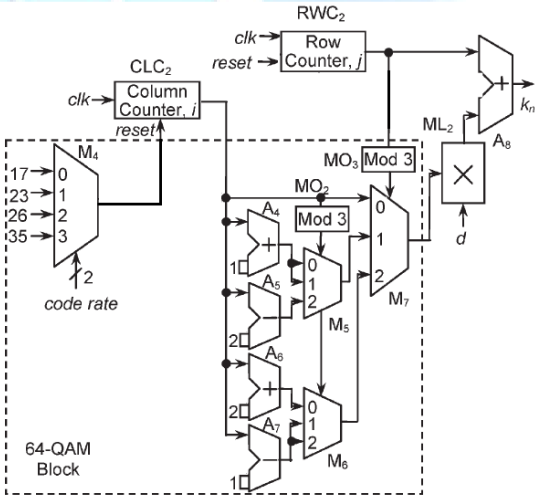


Fig.3. (a) Hardware structure of the address generator for QPSK.



(b) Hardware structure of address generator for 16-QAM.

The design procedure used in 16-QAM is extended in 64-QAM to meet this requirement with the use of additional hardware and is shown in Fig. 3(c). A simple up-counter generates the read addresses for the 2-D deinterleaver.



(c) Hardware structure of address generator for 64-QAM.

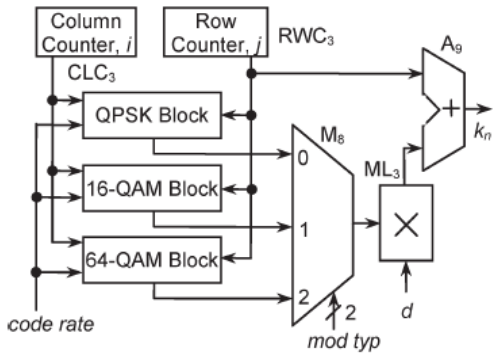


Fig 4.Deinterleaver address generator

The top-level structure of the deinterleaver address generator is shown in Fig. 4. Logic circuits shown inside the dashed line in Fig. 3(a)–(c) are presented here as QPSK block, 16-QAM block, and 64-QAM block, respectively. Our design is optimized in the sense that common logic circuits such as multiplier, adder, row counter, and column counter are shared while generating addresses for any modulation type. In addition, the design also shares the incrementer and the decrementer required in 16-QAM and 64-QAM blocks.

III. IMPLEMENTATION

The proposed hardware model of WiMAX deinterleaver is implemented and tested on Xilinx Spartan-3 (Device: XC3S400) FPGA platform in the laboratory. The FPGA implementation of the interleaver is carried out in two phases; firstly the address generator and thereafter the complete Deinterleaver and presented accordingly.

The Verilog program developed for the proposed WiMAX deinterleaver address generator is downloaded on the Xilinx Spartan-3 (Device XC3S400) FPGA.

IV. SIMULATION RESULT & SNAPSHOTS

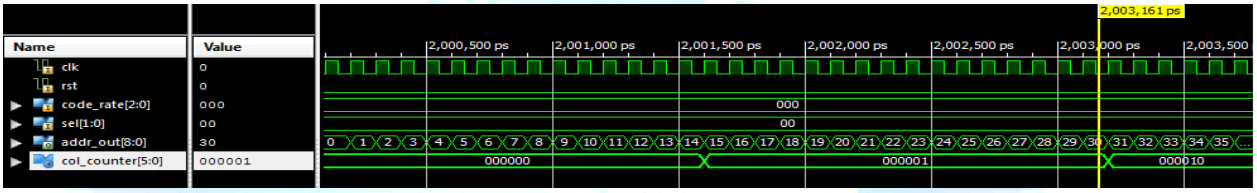
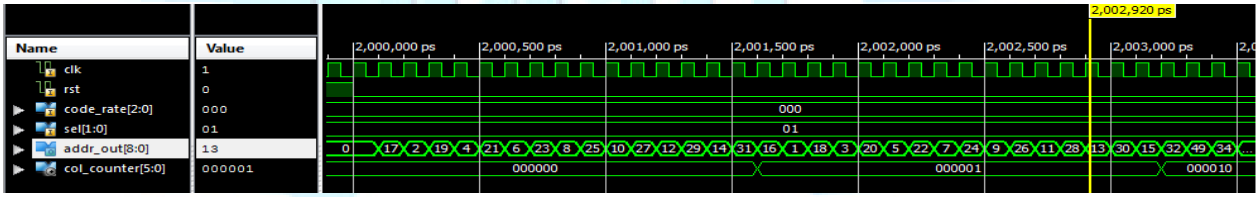
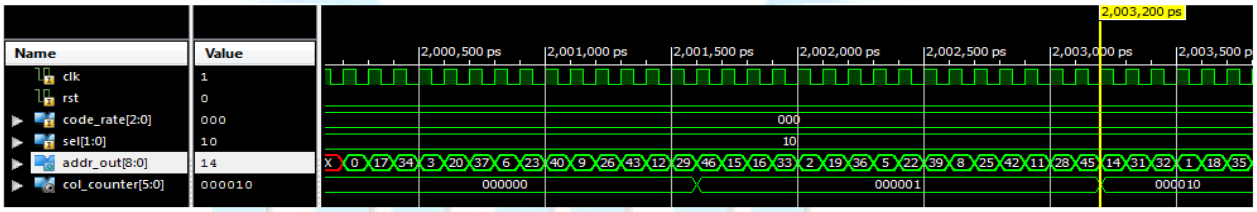


Fig.5 (a). Simulation result showing the addresses for the QPSK Modulation Technique



(b). Simulation result showing the addresses for the QPSK Modulation Technique



(c). Simulation result showing the addresses for the QPSK Modulation Technique

The proposed hardware of the address generator is converted into a Verilog program using the Xilinx ISE. Simulation results are obtained for all permissible modulation types and code rates using ISIM Simulator and some of the snapshots of the result for different N_{cbps}, for different code rate and for different Modulation techniques are shown in Fig.5. The waveforms in Fig. 5(a) – (c) are for the address generator for QPSK, 16 QAM and 64-QAM Methods respectively.

Table III shows the Performance comparison between the proposed, previous and LUT based Technique.

Table III
Comparison between the Proposed, Previous and LUT Based Technique

FPGA Parameters	Performance of the proposed Technique	Performance of the Previous Technique	Performance of the LUT based Technique	% Reduction/ Improvement in resource utilization	
				Previous Technique	Proposed Technique
Slices	0.306 %	3.49 %	17.66	-80.24	-98.27
4 input LUTs	0.265 %	3.35 %	17.15	-80.47	-98.45
Operating Frequency	170.219 MHz	121.82MHz	62.51MHz	48.69	63.27

V. CONCLUSION

This paper presents a technique to implement the Address Generator for WiMAX 2D Deinterleaver on FPGA platform. The presented circuit supports all the code rates and modulation schemes permitted under IEEE 802.16e standard. The simulation results support the correct operation as far as generation of Deinterleaver addresses for WiMAX technology is concerned. The innovation of our approach includes higher operating frequency and better resource utilization in FPGA.

REFERENCES

[1] Bijoy Kumar Upadhyaya, Salil Kumar Sanyal," Efficient FPGA Implementation of Address Generator for Wimax Deinterleaver", IEEE Transaction,Vol. 60,no.8,August 2013

[2] W. Konhauser, "Broadband wireless access solutions—Progressive challenges and potential value of next generation," *Wireless Pers. Commun.*,vol. 37, no. 3/4, pp. 243–259, May 2006.

[3] B. Li, Y. Qin, C. P. Low, and C. L. Gwee, "A survey on mobile WiMAX," *IEEE Commun. Mag.*, vol. 45, no. 12, pp. 70–75, Dec. 2007.

[4] Y. N. Chang and Y. C. Ding, "A low-cost dual mode de-interleaver design,"in *Proc Int. Conf. Consum. Electron.*, 2007, pp. 1–2.

[5] A. A. Khater, M. M. Khairy, and S. E.-D. Habib, "Efficient FPGA implementation for the IEEE 802.16e interleaver," in *Proc. Int. Conf. Microelectron.*, Marrakech, Morocco, 2009, pp. 181–184.

[6] B. K. Upadhyaya, I. S. Misra, and S. K. Sanyal, "Novel design of address generator for WiMAX multimode interleaver using FPGA based finite state machine," in *Proc. 13th Int. Conf. Comput. Inf. Technol.*, Dhaka, Bangladesh, 2010, pp. 153–158.